## REMARKS

The Examiner indicated claims 3-8, 11-16 an19-20 are objected to as being dependent upon an allegedly rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicants gratefully acknowledge the Examiner's indication of allowable subject matter.

The Examiner rejected claims 1-2, 9-10 and 17-18 on the ground of non-statutory obviousness-type double patent as allegedly being unpatentable over claims 1-2 and 7 of U.S. Patent No. 6,928,377.

Applicants respectfully traverse the double patent rejection with the following arguments.

**Double Patenting**

The Examiner rejected claims 1-2, 9-10 and 17-18 on the ground of non-statutory obviousness-type double patent as allegedly being unpatentable over claims 1-2 and 7 of U.S. Patent No. 6,928,377.

Applicants respectfully contend that claims 1, 9, and 17 are not obvious over claims 1-2 and 7 of U.S. Patent No. 6,928,377, because claims 1-2 and 7 of U.S. Patent No. 6,928,377 do not teach or suggest every feature of claims 1, 9, and 17.

A first reason why claims 1, 9, and 17 are not obvious over claims 1-2 and 7 of U.S. Patent No. 6,928,377 is that claims 1-2 and 7 of U.S. Patent No. 6,928,377 do not teach or suggest the feature: "wherein the BIST circuit is configured to perform a first test pass for the first memory circuit **to collect the cycle numbers of failing cycles** for the first memory circuit in response to the first memory circuit being selected for testing" (emphasis added) as recited in claim 1 and similarly in claims 9 and 17.

The Examiner argues that "counting the number of unique failing row addresses of the tested data is effectively the same as counting the number of failing cycles".

In response, Applicants respectfully point out that claims , 9, and 17 do not recite "counting the number of failing cycles" as the Examiner alleges. In fact, nothing is being "counted" in claims 1, 9, and 17. Rather, claims 1, 9, and 17 recite "to collect the cycle numbers of failing cycles". For example, if the cycle numbers of the failing cycles are cycle numbers 2, 4, and 5, then claims 1, 9, and 17 recite collecting cycle number 2, 4, and 5. The number of failing cycles in the preceding example is 3 (i.e., there are 3 failing cycles, namely failing cycles 2, 4,

and 5). Therefore, based on the Examiner's analysis, claims 1-2 and 7 of U.S. Patent No. 6,928,377 disclose the number of failing cycles, namely 3.

In summary in the preceding example, claims 1, 9, and 17 recite collecting cycle numbers 2, 4, and 5, whereas claims 1-2 and 7 of U.S. Patent No. 6,928,377 discloses counting the number (3) of failing cycles.

Therefore, Applicants respectfully maintain that the preceding argument by the Examiner in support of the Examiner's contention that claims 1, 9, and 17 are obvious over claims 1-2 and 7 of U.S. Patent No. 6,928,377 is not persuasive.

A second reason why claims 1, 9, and 17 are not obvious over claims 1-2 and 7 of U.S. Patent No. 6,928,377 is that claims 1-2 and 7 of U.S. Patent No. 6,928,377 do not teach or suggest the feature: "wherein, during a second test pass for the first memory circuit performed by the BIST after the first test pass for the first memory circuit, the BIST circuit is configured **to collect the contents of the locations in the first memory circuit associated with the failing cycles for the first memory circuit**" (emphasis added) as recited in claim 1 and similarly in claims 9 and 17.

The Examiner argues that "if the error count value of the unmasked data column exceeds a previously stored high error count value from previously tested data columns, then the unmasked data column is determined to be the worst data column so far, and the error count for the unmasked data column is stored in an error count register, and a bit-address for the unmasked data column is stored in a repair register is the same as collecting the data and storing it elsewhere."

In response, Applicants respectfully assert that storing an address of the unmasked data column is not the same as collecting or storing the failing data in the unmasked data column. Consider an example in which given memory location has an address A and contains data D. Claims 1, 9, and 17 recite storing D, whereas claims 1-2 and 7 of U.S. Patent No. 6,928,377 disclose storing A. Applicants respectfully assert that A is most certainly not the same as D.

In addition, Applicants respectfully point out that there is no motivation in claims 1-2 and 7 of U.S. Patent No. 6,928,377 to "collect the contents of the locations in the first memory circuit associated with the failing cycles for the first memory circuit" as required by claims 1, 9, and 17, because claim 1 is directed to replacing failed data rather that to collecting failed data. See claim 1 of U.S. Patent No. 6,928,377 ("allocating the spare column to replace the worst failing column"; "allocating the spare rows to replace the failing rows"). In other words, claims 1-2 and 7 of U.S. Patent No. 6,928,377 appear to be saving the addresses of columns/rows in order to replace the data in the columns/rows and not for the purpose of collecting or storing the data in the columns/rows.

Therefore, Applicants respectfully maintain that the preceding argument by the Examiner in support of the Examiner's contention that claims 1, 9, and 17 are obvious over claims 1-2 and 7 of U.S. Patent No. 6,928,377 is not persuasive.

Based on the preceding arguments, Applicants respectfully contend that claims 1, 9, and 17 are not obvious over claims 1-2 and 7 of U.S. Patent No. 6,928,377 and that claims 1, 9, and 17 are in condition for allowance. Since claim 2 depends from claim 1, Applicants respectfully contend that claim 2 is likewise in condition for allowance. Since claim 10 depends from claim

9, Applicants respectfully contend that claim 10 is likewise in condition for allowance. . Since claim 18 depends from claim 17, Applicants respectfully contend that claim 18 is likewise in condition for allowance.

In addition with respect to claims 2, 10, and 17, Applicants respectfully contend that claims 1-2 and 7 of U.S. Patent No. 6,928,377 do not teach or suggest the feature: " wherein the BIST circuit further comprises a memory circuit select register configured to receive a select value via scanning such that the first memory circuit is selected for testing" as recited in claim 2 and similarly in claims 10 and 17.

The Examiner argues that "using a multiplexor is recognized is an art recognized equivalent of a selector".

In response, Applicants respectfully contend that a "multiplexor" is not recited anywhere in claims 1-2 and 7 of U.S. Patent No. 6,928,377.

Moreover, even if claims 1-2 and 7 of U.S. Patent No. 6,928,377 did recite a "multiplexor" (which claims 1-2 and 7 of U.S. Patent No. 6,928,377 do not do), the Examiner would be required to demonstrate that said multiplexor is "configured to receive a select value via scanning such that the first memory circuit is selected for testing", which the Examiner has not even addressed.

Therefore, Applicants respectfully maintain that the preceding argument by the Examiner in support of the Examiner's contention that claims 2, 10, and 17 are obvious over claims 1-2 and 7 of U.S. Patent No. 6,928,377 is not persuasive.

In addition with respect to claim 18, Applicants respectfully contend that claims 1-2 and 7 of U.S. Patent No. 6,928,377 do not teach or suggest the feature: "using a data-out register in the RAM to store the content of a location in the RAM associated with the cycle". The Examiner has not provided any evidence to allegedly show that claims 1-2 and 7 of U.S. Patent No. 6,928,377 teach the preceding feature of claim 18.

In addition with respect to claim 18, Applicants respectfully contend that claims 1-2 and 7 of U.S. Patent No. 6,928,377 do not teach or suggest the feature: "using a comparator in the RAM to compare the content of the data-out register and an expected value from the BIST circuit and to generate a fail signal if the content of the data-out register and the expected value are not equal". The Examiner has not provided any evidence to allegedly show that claims 1-2 and 7 of U.S. Patent No. 6,928,377 teach the preceding feature of claim 18.

In addition with respect to claim 18, Applicants respectfully contend that claims 1-2 and 7 of U.S. Patent No. 6,928,377 do not teach or suggest the feature: "using a mode multiplexer to pass the fail signal from the comparator to a chip multiplexer". The Examiner has not provided any evidence to allegedly show that claims 1-2 and 7 of U.S. Patent No. 6,928,377 teach the preceding feature of claim 18.

In addition with respect to claim 18, Applicants respectfully contend that claims 1-2 and 7 of U.S. Patent No. 6,928,377 do not teach or suggest the feature: "using the chip multiplexer to pass the fail signal from the mode multiplexer to a tester outside the memory chip". The

Examiner has not provided any evidence to allegedly show that claims 1-2 and 7 of U.S. Patent No. 6,928,377 teach the preceding feature of claim 18.

## CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If the Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invites the Examiner to contact Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0457.

Date: 01/30/2007

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